A Scalable General-Purpose Model for Microwave FET's Including DC/AC Dispersion Effects

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***Abstract*— This paper addresses the issue of scalability in equivalent circuit-based models for FET's, emphasizing for the first time the particularly difficult problems associated with the scalability of dc/ac dispersion phenomena. A study has been carried out on devices from both MESFET ($L_G = 0.5$ μm) and pseudomorphic high electron-mobility transistor (PHEMT) ($L_G = 0.2$ μm) foundry processes, with total gatewidths between 60–1200 μm. Results are presented, showing that at least up to medium-size devices, dc characteristics, and most of the bias-dependent small-signal circuit elements scale in general, very well provided a reliable parameter extraction methodology is implemented. However, in the case of dispersion phenomena, while the differential dc/ac transconductance obeys straightforward scaling rules, the output conductance does not. The main features of a general-purpose scaleable microwave FET model—*COBRA*—are described. This includes an equivalent circuit-based solution to account for dispersion effects. The solution is compact, obeys the required conservation constraints, and can "absorb" the scaling inconsistencies observed in the output conductance. The corresponding modeling methodology is also described. Finally, a comprehensive set of measurement versus simulation scalability test results are presented, including dc, small-signal, and large-signal tests.**

***Index Terms*— Microwave FET's, microwave transistors, nonlinear modeling, parameter extraction, semiconductor device modeling.**

I. Introduction

DESPITE intense studies in recent years into the problem of nonlinear microwave FET modeling, the issue continues to cause concern to microwave and RF design engineers, as it remains one of the major sources of errors in MMIC design. While significant progress has been achieved in some areas of the field, there are still some important aspects that have been traditionally sidelined, such as scalability and yield analysis. The issue of model scalability is of prime importance, particularly to design engineers working in monolithic-microwave integrated-circuit (MMIC) foundries, who have to deal with circuits of increasing complexity, and need to have the flexibility and confidence to use a wide range of device sizes in their designs. Consequently, for them, the availability of very accurate device models without correspondingly good scaling qualities, makes little practical sense. Most of the available models are lacking in this area, either by ignoring the issue altogether or by not addressing some of the more difficult aspects, such as the scalability of dispersion effects.

In this paper, we present results from a recent study carried out on some FET foundry processes, both MESFET and pseudomorphic high electron-mobility transistor (PHEMT) from different manufacturers, regarding among other aspects, the scalability of a general-purpose model for microwave FET's. In general, scalability presents particular difficulties in equivalent circuit-based and black-box modeling approaches, since geometrical dimensions do not explicitly appear in the model structure. In the case of equivalent circuit-based models, our study showed that up to medium-size devices, most of the important equivalent circuit elements can be scaled using straightforward linear rules. However, we have found that there are some second-order phenomena, i.e., the dc/ac dispersion of the output conductance, that do not obey these simple scaling rules. This is likely to generate even more difficulties in finding a solution to the scalability problem, within most of the modeling approaches currently in use. A robust and relatively straightforward empirical equivalent circuit solution and the associated modeling methodology are introduced.

In Section II, we briefly present the most important features and strengths of the general-purpose scaleable *COBRA* model for microwave FET's. In Section III, we describe some of the findings from our study, related to the scaling inconsistencies observed in the differential dc/ac transconductance and output conductance. An equivalent circuit solution to account for the nonlinear dispersive effects and the corresponding modeling methodology are described in Section IV. Finally, in Section V, as well as in the previous sections, a wide range of test results are presented, comparing experimental data with simulation results.

II. *COBRA*: A General-Purpose Scalable FET Model

This model belongs to the category of nonlinear equivalent circuit models. A comprehensive and robust parameter extraction methodology has been developed in connection with the model. The general topology of the FET equivalent circuit model, including the parasitic elements, is presented in Fig. 1 and, apart from the rather more complex structure of the drain circuit, it is seen to be very similar to the topology assumed by other commonly used models. However, *COBRA* stands out with respect to other similar models through a number of novel features and strengths which are briefly described below.

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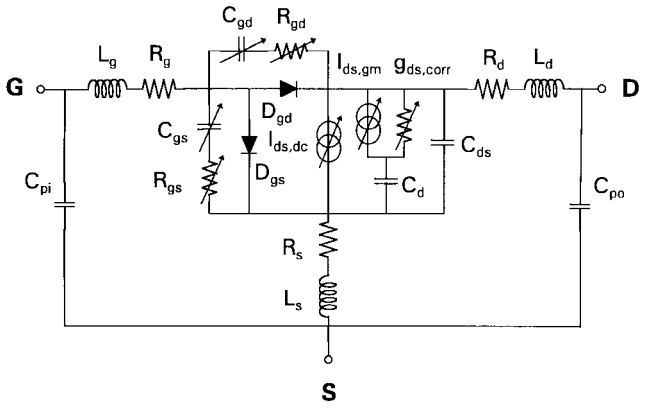


Fig. 1. A general-purpose equivalent circuit model (*COBRA*) for microwave FET's, accounting for dispersion phenomena.

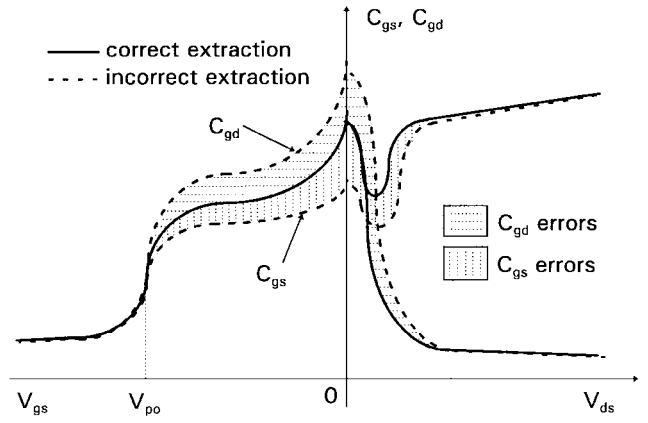


Fig. 2. Illustration of the common errors encountered when extracting the intrinsic gate capacitances, due to faulty values determined for the parasitic resistances.

A. Parameter Extraction

Parameter extraction of equivalent circuit nonlinear models for microwave FET's has been an area well covered by researchers over the years and it is fair to say that it has reached a certain level of maturity. Several approaches have been proposed in relation to the extraction of the parasitic elements [1]–[4], most of them based on a combination of dc and small-signal S-parameters measured under certain special bias conditions. As far as the de-embedding of parasitics and the extraction of the intrinsic elements is concerned, the very elegant method proposed by Dambrine *et al.* [1], and further improved by Berroth and Bosch [2], is well established and very efficient. It is, however, interesting that many device manufacturers still complain about problems and inconsistencies when these extraction techniques are applied in practice. One important and persistent complaint regards the frequently observed presence of very significant bias-dependent asymmetries between the gate-to-source and gate-to-drain capacitances (Fig. 2) extracted at $V_{\rm ds} = 0$ [4]. This is in contrast to the relative symmetrical geometry presented by the large majority of FET devices, under these particular bias conditions. The consequences can be serious from a modeling point of view, and designs based on these models can be badly affected, especially in applications such as mixers and switches.

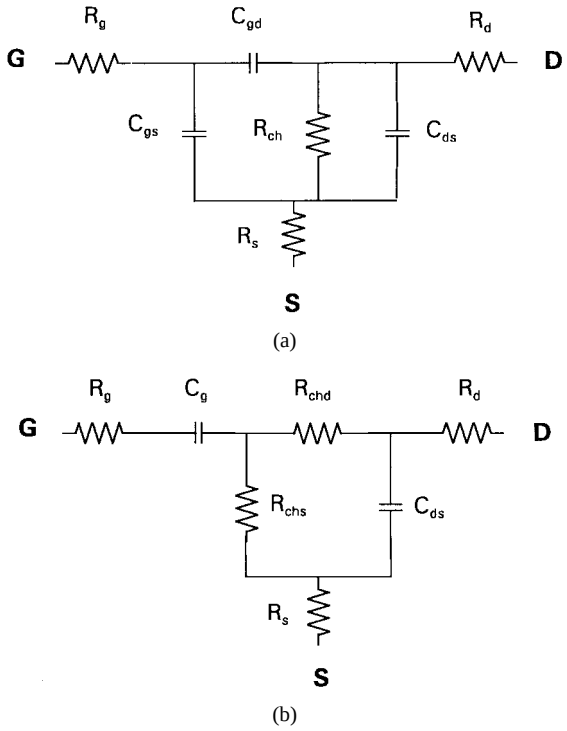


Fig. 3. Simplified FET equivalent circuit model topologies commonly used for parasistic extraction. (a) "Below pinchoff" case. (b) "Above pinchoff" case.

Most of the techniques employed to extract the parasitic elements of a microwave FET are based upon small-signal S-data or dc data, measured at $V_{\rm ds} = 0$. The main reason is that under these conditions the equivalent circuit model can be simplified to a great extent. Furthermore, one of the factors which allows this simplification is the relative symmetry of the active channel under these bias conditions, determined mainly by the symmetry of the depletion region under the gate. The small geometrical asymmetries that exist normally between the source and drain contacts relative to the gate are not likely to have a significant impact in this case. The circuit topologies commonly used for parasitic extraction differ between the "below pinchoff" case [Fig. 3(a)] and the "above pinchoff" case [Fig. 3(b)]. The partitioning rule for these resistances is normally chosen as follows:

$$R_{\rm chs} = \alpha R_{\rm ch} \quad R_{\rm chd} = (1-\alpha) R_{\rm ch} \tag{1}$$

where $R_{\rm ch}$ is the total channel resistance and α has a value that varies from author to author, between 0.33–0.5. It is quite obvious that if the balance between those two resistances (i.e., the value of α) is incorrect, the values determined for the source and drain resistances will be affected.

Although perhaps more convenient, there are a couple of disadvantages associated with the second topology. Firstly, it is not consistent with the topology used in all the other circumstances (below pinchoff and under normal bias conditions), which involves two gate capacitances. Secondly, it carries with it an uncertainty related to the balance between the two channel resistances $R_{\rm chs}$ and $R_{\rm chd}$.

Within the extraction methodology associated with the *COBRA* model, the parasitic resistances are determined using solely the "unbiased" and "pinched-off" FET S-data. The same

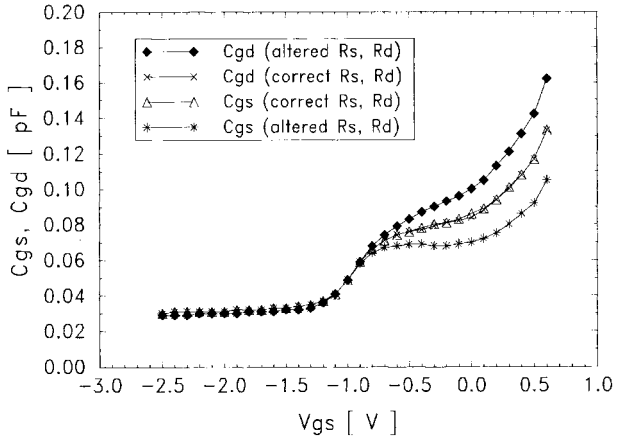


Fig. 4. Example of extracted gate capacitances at $V_{\rm ds} = 0$, for a 120-μm PHEMT considering two sets of values for R_s and R_d. In the first case, with the correct values it is seen how the two gate capacitances are essentially identical, as expected. In the second case, the value of R_d has been altered from 0.79 to 1.2 Ω, and the capacitance extraction has been repeated. The result shows major differences between the two gate capacitances above pinchoff.

"Π" topology [Fig. 3(a)] is used to model the FET in both these bias conditions. For low enough frequencies ($f < 10$ GHz, where $\omega R_{\rm cli} C \ll 1$), the "$\Pi$" structure $C_{\rm gs}$–$C_{\rm gd}$–$R_{\rm cli}$ can be related to the "$\mathbf{T}$" structure C_g–$R_{\rm clis}$–$R_{\rm clid}$ [Fig. 3(b)] by comparing the input and output $\mathbf{Z}$ parameters of the two configurations [4]. This method returns a value of 0.25 for the parameter α. With this value, we can now use the "$\mathbf{T}$" topology and the technique described in [5] to determine R_s and R_d. Another very important aspect is the frequency range where the extraction of R_g, R_s, and R_d is carried out. The frequency dependence of these elements should be monitored during the extraction process, as it tends to vary from one process to another. The frequency range should be chosen so that the impact of inductive and/or capacitive reactances in the circuit is minimum.

The intrinsic elements are extracted using the classical small-signal equivalent circuit model topology for FET's, with both charging resistances $R_{\rm gs}$ and $R_{\rm gd}$ included, and using for extraction a technique based on that described in [2]. Again, the frequency range where the extraction is carried out is very important, and different frequency ranges might be needed to extract different parameters. In Fig. 4 is an example of how, by implementing such an extraction methodology, we reduce the risk for errors of the type commonly encountered in the extraction of gate capacitances above pinchoff and around $V_{\rm ds} = 0$. More examples of that kind can be found in [4].

Regarding the scalability properties of a model, it has to be emphasized that the choice of a model circuit topology together with the parameter extraction methodology used are crucially important. The closer the parameter values returned by the extraction process are to the correct ones, the greater the chances that the model will scale well. Having said that, we will see further that these are only necessary conditions for good scalability, but they are not sufficient. To illustrate the efficiency of our extraction methodology, in Fig. 5(a) and (b) we compare, for two of the most important bias-dependent small-signal elements of the equivalent circuit model, the values

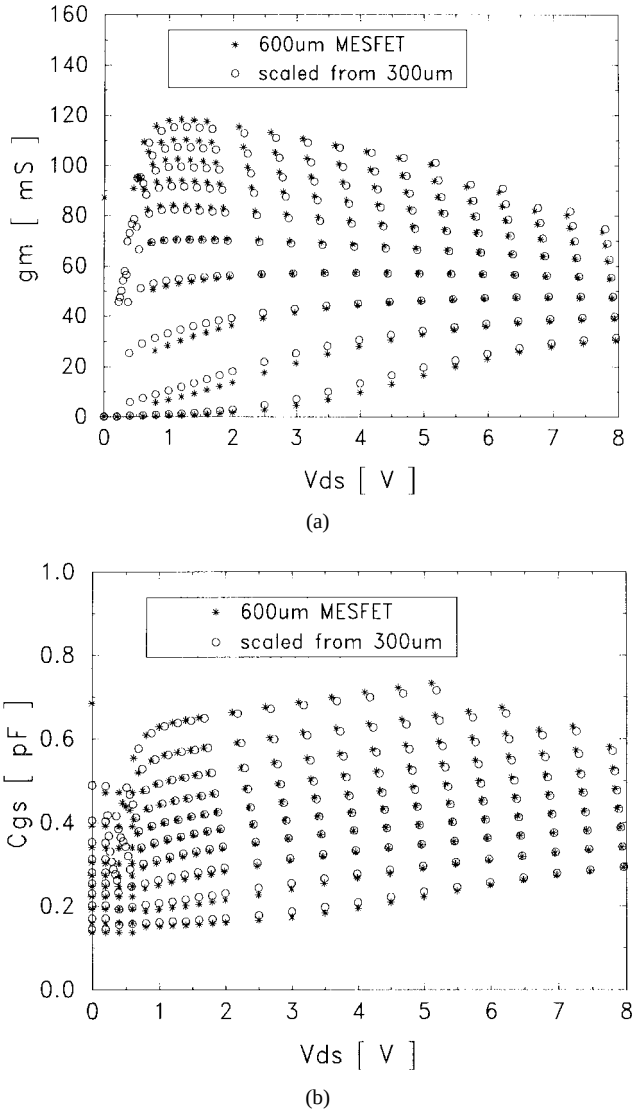


Fig. 5. Illustration of good scaling properties of the extracted multibias small-signal intrinsic elements. The results are determined from a 0.5 × (4 × 150) μm MESFET and compared with those scaled from a 0.5 × (4 × 75) μm MESFET. (a) Transconductance. (b) Gate-to-source capacitance ($V_{\rm gs} = -1.2$ V to $+0.6$ V; $V_{\rm po} = -1.1$ V).

extracted directly for a 600-μm MESFET with those obtained via a simple scaling process from a 300-μm MESFET. The scaling properties are seen to be very good across the whole bias range.

B. DC Model

The two diodes in the gate circuit are adequately described by the classical Schottky diode *I–V* law. Results in Fig. 6 illustrates good scalability properties of such representation for three different device sizes (area ratios 1:2:4) from the MESFET process.

The nonlinear model function implemented for the drain current (2) describes very well the FET behavior all around the bias spectrum: linear, knee, and the saturation regions; reverse bias region; it can also describe soft breakdown and mild second knee behavior; it converges smoothly toward zero, when $V_{\rm gs}$ drops below pinchoff; has the ability to follow the

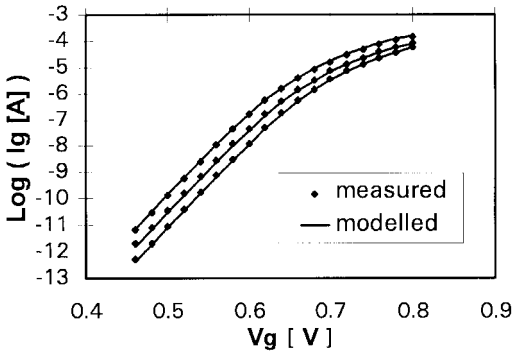


Fig. 6. Scalability of the gate current model (illustrated for 300-, 600-, and 1200-μm MESFET's).

negative slope seen in real FET's in the saturation region at high values of the gate voltage due to electron traps and self-heating effects. The equations are

$$I_{\mathrm{ds,DC}} = \beta \cdot V_{\mathrm{eff}}^{\frac{\lambda}{\sqrt{1+\mu \cdot V_{\mathrm{ds}}^2}+\xi \cdot V_{\mathrm{eff}}}} \cdot \tanh[\alpha \cdot V_{\mathrm{ds}} \cdot (1+\zeta \cdot V_{\mathrm{eff}})]$$
$$V_{\mathrm{eff}} = \frac{1}{2} \cdot \left(V_{\mathrm{gst}} + \sqrt{V_{\mathrm{gst}}^2 + \delta^2}\right)$$
$$V_{\mathrm{gst}} = V_{\mathrm{gs}} - (1+\beta r^2) \cdot V_{T0} + \gamma \cdot V_{\mathrm{ds}} \quad (2)$$

where V_{T0} is the pinchoff voltage and α, β, β_r, γ, δ, λ, μ, ξ, ζ are model parameters, and β_r is a dimensionless parameter, numerically equal with β (when I_{ds} is expressed in amperes). The model function is continuous over the entire bias plane and its derivatives are continuous, which is very important for a good representation of the intermodulation characteristics. In Fig. 7(a) and (b), the dc model is compared with the measured data for two PHEMT devices (area ratio 1:10). The results are showing that the model still works well, even for very large-size devices. Its scalability is ensured by applying simple scaling rules to four of the model parameters: β (and implicitly β_r), γ, μ, and δ. Up to medium-size devices, the scaling accuracy remains very good even if only two of the model parameters are scaled.

C. Other Nonlinear Elements

Suitable nonlinear functions are available for other nonlinear elements in the equivalent circuit model, which are traditionally considered constant or ignored altogether, such as the charging resistances. New gate capacitance model functions are also provided and the model extraction technique, similar to the one described in [5], ensures that the two gate capacitances are identical at $V_{\mathrm{ds}} = 0$. The charge conservation problem has been taken into account in the preliminary implementation of the model in HP-MDS, through the appropriate use of a nonlinear symbolically defined device (SDD) element.

III. Scalability of Dispersion Effects

We have determined the differences between the dc and the small-signal transconductances and output conductances for a number of PHEMT and MESFET foundry devices with the total gatewidth varying between 60–1200 μm. As

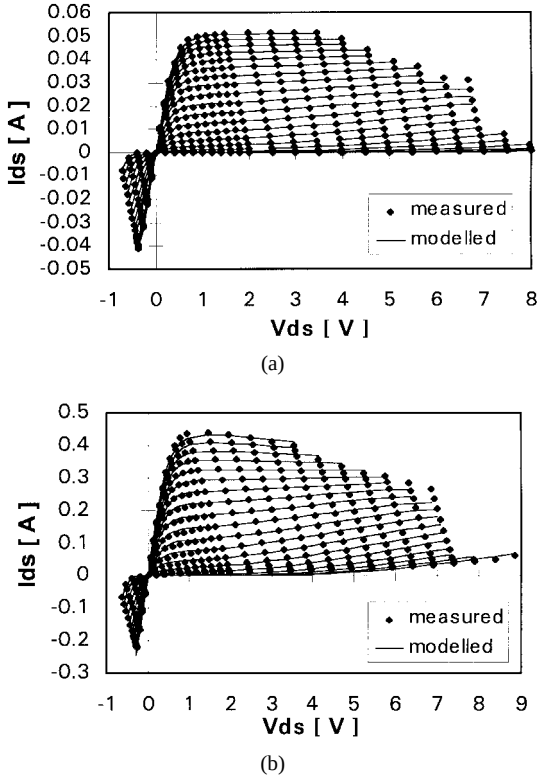


Fig. 7. Scalability of *COBRA* dc model (area ratio 1:10). (a) Model applied to a 0.2 × (4 × 30) μm PHEMT. (b) Model scaled to a 0.2 × (6 × 200) μm PHEMT (four model parameters have been scaled).

a general rule, it has been observed that the differential dc/ac transconductances follow a straightforward scaling pattern, as shown in a typical example in Fig. 8(a) and (b). However, in the case of the output conductances the scaling pattern is found to be significantly different. To better emphasise this phenomenon, we have calculated the relative errors in estimating the differential dc/ac conductances when straightforward scaling rules are employed as follows:

$$g_{m,\mathrm{diff\_err}} = \frac{g_{m,\mathrm{diff}} - g_{m,\mathrm{diff\_sc}}}{g_m} \cdot 100\,[\%]$$
$$g_{\mathrm{ds,diff\_err}} = \frac{g_{\mathrm{ds,diff}} - g_{\mathrm{ds,diff\_sc}}}{g_{\mathrm{ds}}} \cdot 100\,[\%] \quad (3)$$

where $g_{m,\mathrm{diff}}$ and $g_{\mathrm{ds,diff}}$ are the differential dc/ac conductances, while $g_{m,\mathrm{diff\_sc}}$ and $g_{\mathrm{ds,diff\_sc}}$ are the differential dc/ac conductances as scaled from a device of a different size. The two relative errors are compared in Fig. 9(a) and (b) for the case of an 120- and 300-μm device. It is seen that the relative error in the case of the differential transconductance remains generally below 3%, whereas in the case of the output conductance, this error is about six to seven times higher. Results compare in similar fashion for the other device sizes tested for this process.

However, this phenomenon seem to be process related, and for that reason it will be very hard to model in a consistent way, regardless of what modeling approach is used. For example, a low-power MESFET process also under study showed much less difference between the two relative error quantities described above, whereas for a power MESFET

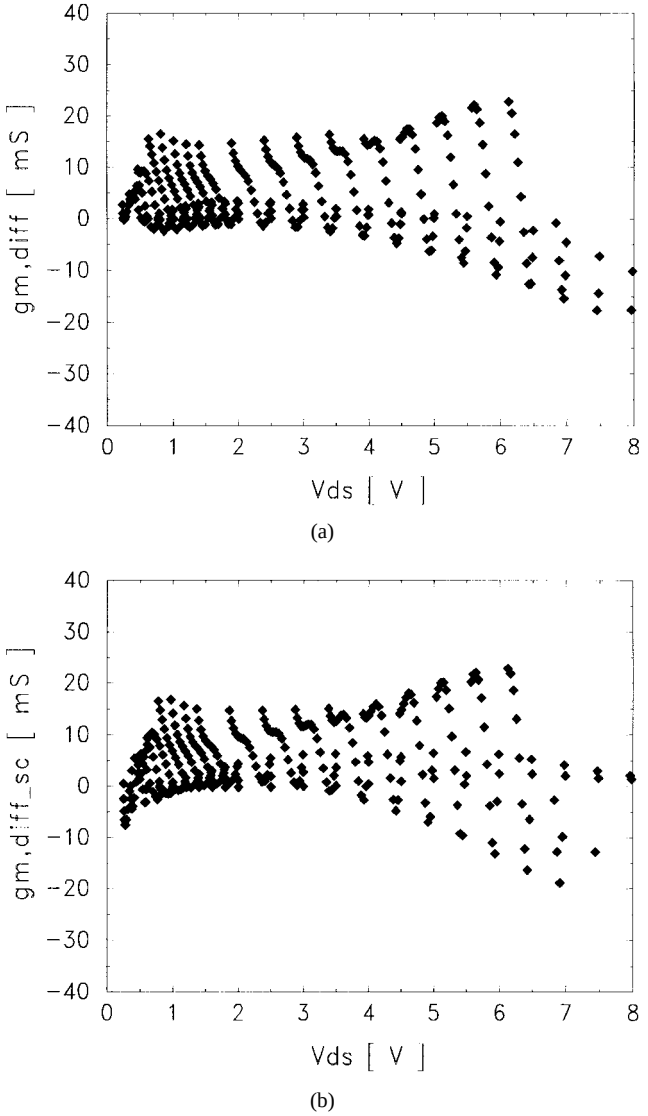


Fig. 8. The differences between dc and small-signal transconductances determined for a 300-μm PHEMT (a) as extracted directly and (b) as scaled from a 120-μm device.

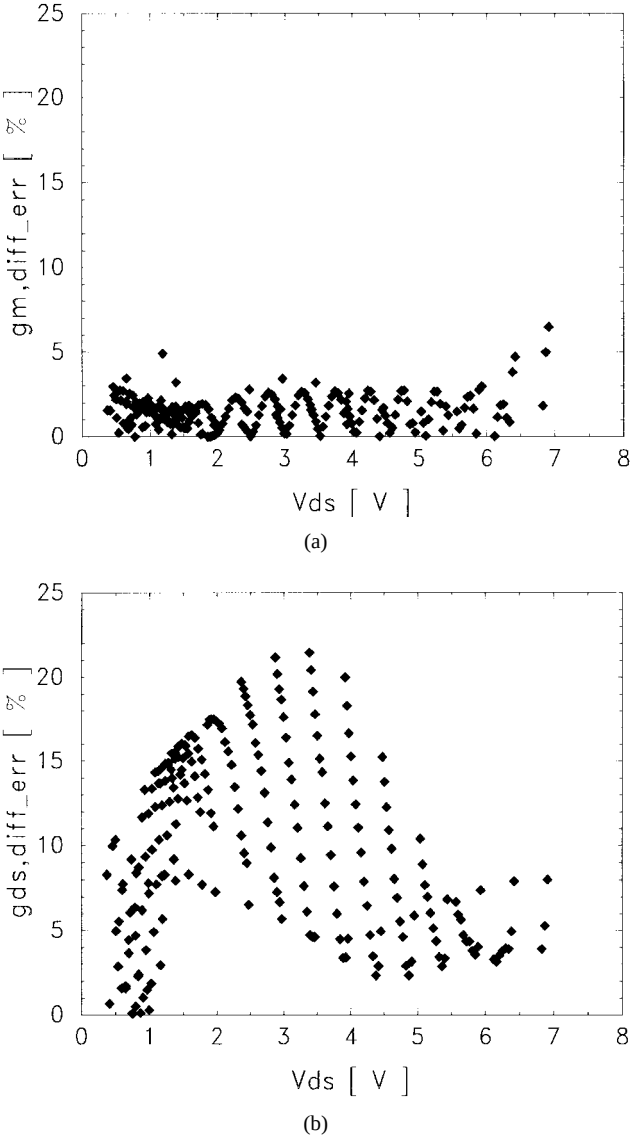


Fig. 9. The relative error computed for the two differential dc/ac conductances in the case of a 300-μm PHEMT between the values determined directly and scaled from a 120-μm device. (a) Differential transconductance error. (b) Differential output conductance error.

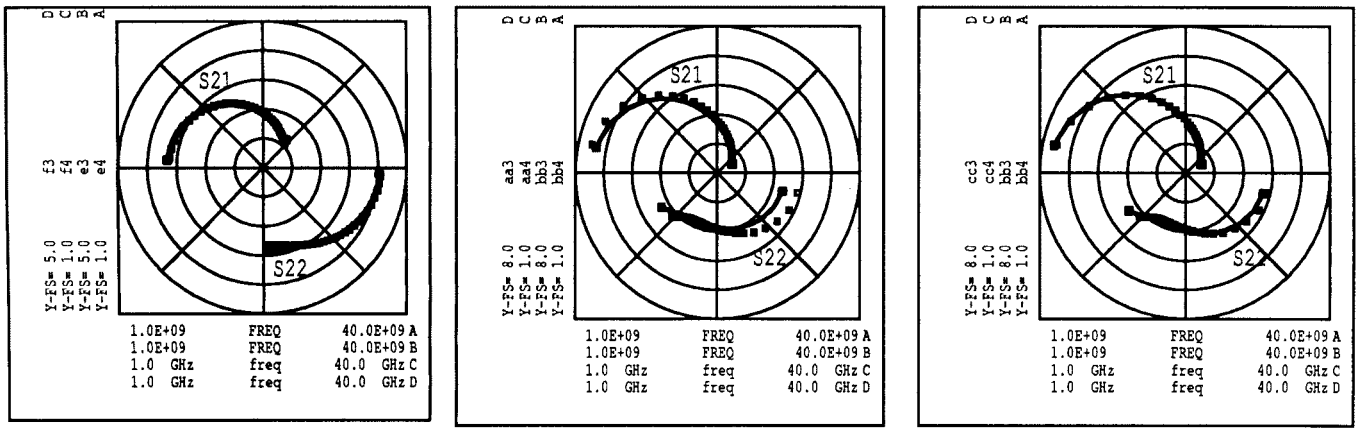
process from the same foundry, those differences were more significant. Such inconsistent behavior is expected to constitute a problem for any type of modeling approach, when it comes to dealing with scalability issues. Possibly the best solution to this problem will be to find a modeling methodology that can "absorb" such behavior for any individual process.

IV. Differential DC/AC Dispersion Modeling Methodology

A number of solutions have been proposed to deal with modeling transconductance and output conductance dispersion in FET's, ranging from a simple *RC* network [6], or an extra ac current source in the drain circuit [7], [16] within traditional equivalent circuit models to the introduction of a correction term in the formulation of the total drain current as a line integral over the differences between dc and small-signal conductances within the most recent look-up table-based models [8]–[10]. In a similar fashion, the total drain current has been defined within so-called conservative FET models [11]. Other approaches, use a combination of supplementary analytical terms added in the drain–current function, with a *RC* network in the drain circuit [14]. Whatever the modeling approach, for a model to be physically sound, the following conservation (or integrability) condition needs to be satisfied, as previously shown in [11], [12]:

$$\frac{\partial(g_m(V_{\rm gs},V_{\rm ds})-g_{m,{\rm DC}}(V_{\rm gs},V_{\rm ds}))}{\partial V_{\rm ds}} = \frac{\partial(g_{\rm ds}(V_{\rm gs},V_{\rm ds})-g_{{\rm ds},{\rm DC}}(V_{\rm gs},V_{\rm ds}))}{\partial V_{\rm gs}}. \tag{4}$$

The two circuit model solutions mentioned above, although giving reasonable results in many situations, do not identically satisfy (4).



(a) (b) (c)

Fig. 10. Comparison between measured and simulated $S21$ and $S22$ using *COBRA* model (a) for a 120-μm PHEMT, (b) scaled to a 300-μm PHEMT (using straightforward scaling rules), and (c) scaled to a 300-μm PHEMT (using specific scaling rule for $g_{\mathrm{ds,corr}}$).

A way to correct this is by employing a circuit model as seen in Fig. 1, where the elements in the drain circuit [13] are determined following a sequence of steps as described below.

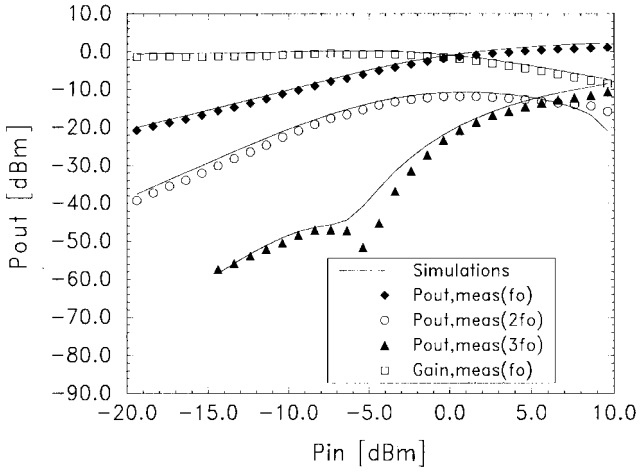
1) $I_{\mathrm{ds,DC}}$ is simply determined by fitting the dc model function on the dc data.
2) Differences are found between the small-signal and dc transconductances.
3) $I_{\mathrm{ds,gm}}$ is described by a similar nonlinear function as $I_{\mathrm{ds,DC}}$, but its parameters are determined by fitting a nonlinear function of the form:

$$g_{m,\mathrm{AC}}(V_{\mathrm{gs}}, V_{\mathrm{ds}}) = \frac{\partial}{\partial V_{\mathrm{gs}}} I_{\mathrm{ds,DC}}(V_{\mathrm{gs}}, V_{\mathrm{ds}}) \qquad (5)$$

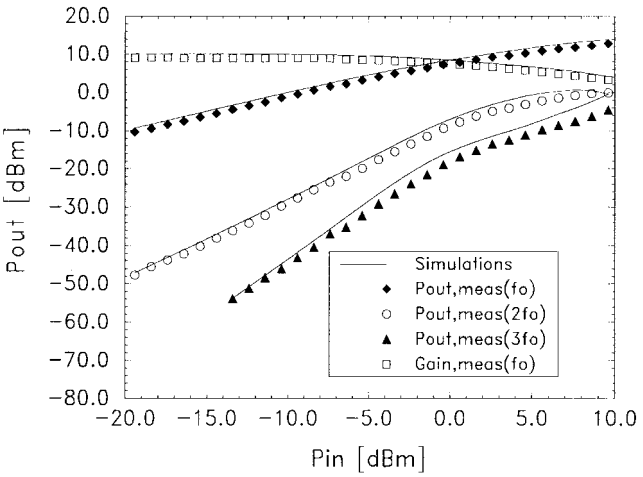
   to the data calculated in step two.
4) Differences are calculated between the small-signal output conductance and the output conductance determined by $I_{\mathrm{ds,DC}}$ and $I_{\mathrm{ds,gm}}$ combined.
5) The nonlinear conductance $g_{\mathrm{ds,corr}}$ is determined by fitting the data determined in step four to an appropriate empirical nonlinear function.
6) The capacitor C_d can be implemented as a nonlinear element and its value can be determined from pulsed dc measurements. However, our experience shows that for the large majority of applications of practical interest, as a first approximation, allocating a constant value to C_d is very satisfactory.

V. Results

This equivalent circuit modeling solution have been implemented as part of the scalable general-purpose *COBRA* model for microwave FET's. From the modeling technique described above, it is quite clear that the scaling inconsistencies seen in the differential dc/ac output conductance can be accounted for in our model via the additional nonlinear conductance $g_{\mathrm{ds,corr}}$ by an appropriate choice of the empirical function that describes it. As an example, Fig. 10 represents the simulation versus experiment test results of small-signal $S21$- and $S22$-parameters (which are the most likely to be affected by these effects) with the *COBRA* model for a 120- and 300-μm PHEMT's. Fig. 10(a) shows the simulation for the 120-μm device, while Fig. 10(b) and (c) show the simulations with the same model for a 300-μm PHEMT, using straightforward



(a)



(b)

Fig. 11. Single-tone large-signal test results for a 0.2 × (4× 30) μm PHEMT, using the *COBRA* model ($V_{\mathrm{po}} = -1.0$ V). (a) $V_{\mathrm{gs}} = -0.9$ V, $V_{\mathrm{ds}} = +0.6$ V and (b) $V_{\mathrm{gs}} = -0.6$ V, $V_{\mathrm{ds}} = +3.0$ V.

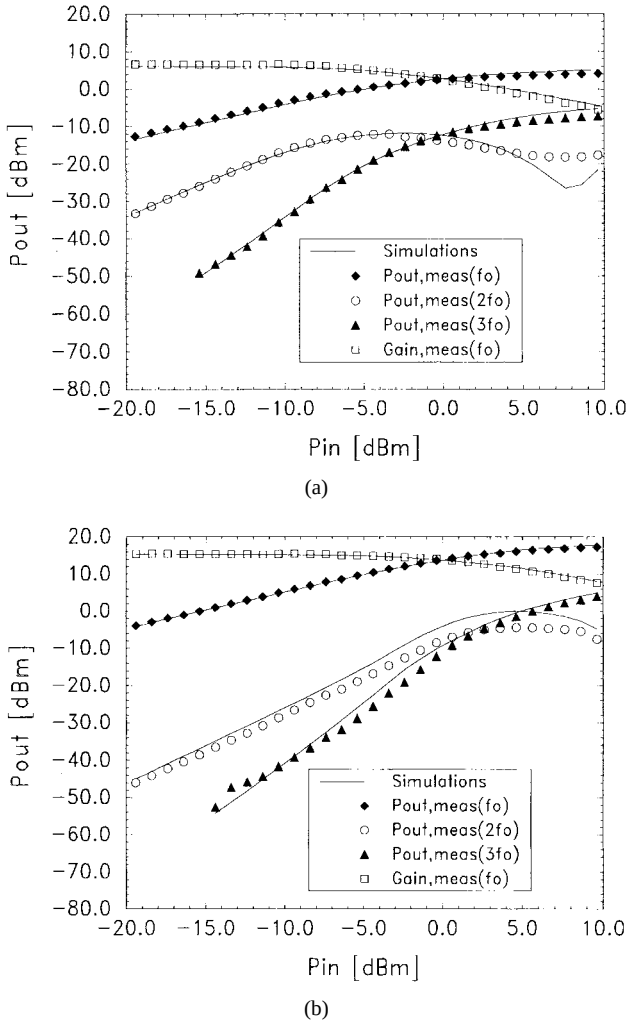


Fig. 12. Single-tone large-signal test results for a 0.2 × (6 × 50) μm PHEMT, using the *COBRA* model scaled from 0.2 × (4 × 30) μm ($V_{\rm po} = -1.0$ V). (a) $V_{\rm gs} = -0.9$ V, $V_{\rm ds} = +0.6$ V and (b) $V_{\rm gs} = -0.6$ V, $V_{\rm ds} = +3.0$ V.

scaling rules for $g_{\rm ds,corr}$ (b), and using a specific scaling rule for $g_{\rm ds,corr}$ (c), respectively. The improvement introduced in the latter case, particularly in $S22$, is quite obvious. In Figs. 11 and 12, the scaling performance of *COBRA* is tested once again, this time in single-tone large-signal tests performed at two bias conditions, for the same two device sizes. Similar small- and large-signal tests have been performed at five different bias conditions, and more of these results can be found in [15].

VI. Conclusion

In this paper, we have shown that accounting for the scalability of dispersive phenomena in microwave FET's models is not trivial. Up to medium-size devices, simple scaling rules apply to most of the equivalent circuit parameters providing that a reliable parameter extraction technique is employed. However, in the case of dispersive phenomena, it appears that differential dc/ac transconductance obeys, with good approximation, straightforward scaling rules, and for differential dc/ac output conductance, such rules are no longer applicable. Quantitatively, this behavior seems to be process dependent. This is likely to create difficulties for most models currently in use, regardless of the modeling approach, if they are to be completed with adequate and accurate scaling features. We have briefly presented the main strengths of a general-purpose scaleable FET model (*COBRA*), which also includes an empirical differential dc/ac dispersion modeling methodology. This solution is compact, complies with the required conservation constraints, and has the flexibility to accommodate the scaling inconsistencies described above. A wide range of test results have been included based on a study carried on both MESFET and PHEMT foundry processes, which emphasize the good scaling capabilities of the *COBRA* model.

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